R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

INTERVIEW SUMMARY

Applicants' representative, John Ignatowski, spoke with Examiner Huynh on May 25, 2005, to discuss the rejections of claims 2-5, 10 and 20. The Examiner noted that in the rejection of claims 2-5 and 10, "Gissel" should read "Schmid" and the missing reference in the rejection of claim 20 is Chan. The claims were not discussed. No samples were presented. No agreement was reached regarding the claims.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 4 lines 2-18, page 9 lines 9-15 and FIGS. 1 and 2, as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-20 under 35 U.S.C. §103(a) as being unpatentable over Chan et al. '505 (hereafter Chan) in view of Schmid et al. '291 (hereafter Schmid) has been obviated in part, is respectfully traversed in part, and should be withdrawn.

Chan concerns a hybrid routing architecture for high density complex programmable logic device (Title). Schmid concerns a virtual private switched telephone network (Title).

Claim 1 provides an assembly apparatus comprising one of (i) a substrate and (ii) a housing. In contrast, one of ordinary skill in the art would not appear to understand any of the elements listed on page 2 of the Office Action ("pc, system, mainboard") to be similar to the claimed substrate or the claimed housing. Furthermore, both Chan and Schmid appear to be silent regarding a substrate or a housing. Therefore, Chan and Schmid, alone or in combination, do not appear to teach or suggest an assembly apparatus comprising one of (i) a substrate and (ii) a housing as presently claimed.

Claim 1 further provides that the programmable logic device and the die are directly mounted to the assembly apparatus. In contrast, Chan does not appear to mention a CPLD 400 (asserted similar to the claimed programmable logic device) being mounted to anything. Likewise, Schmid does not appear to mention the FPGA 518 (asserted similar to the claimed die) mounted to anything. Therefore, Chan and Schmid, alone or in combination, do not appear to teach or suggest a programmable logic device and a die directly mounted to the assembly apparatus as presently claimed.

Claim 1 further provides that the die comprises a first communication channel coupled to a first of a plurality of routing channels (in the programmable logic device) to exchange a first parallel data signal with at least one of a plurality of logic

block clusters (in the programmable logic device). In contrast, Chan appears to be silent regarding a routing channel of the CPLD 400 (asserted similar to the claimed programmable logic device) coupled to any die capable of performing serial/parallel conversions. Furthermore, Schmid appears to be silent regarding a communication channel of the FPGA 518 (asserted similar to the claimed die) coupled to any type of programmable logic device. As such, neither Chan or Schmid appear to teach coupling the routing channel of the CPLD 400 of Chan to a communication channel of the FPGA 518 of Schmid. The only source for teaching such a coupling appears to be applicants' specification and claims which cannot be used to establish the asserted combination. Therefore, Chan and Schmid, alone or in combination, do not appear to teach or suggest that the die comprises a first communication channel coupled to a first of a plurality of routing channels (in the programmable logic device) to exchange a first parallel data signal with at least one of a plurality of logic block clusters (in the programmable logic device) as presently claimed.

Furthermore, no clear and particular evidence of motivation appears to exist to combine the references. The alleged motivation on page 3 of the Office Action to "provide secure access across the untrusted PSTN through telephony resources that can be initiated by a security events" appears to explain why one of ordinary skill in the art would use Schmid instead of conventional interface circuitry to a PSTN. However, the alleged motivation does not appear to explain why one of ordinary skill in the art

would combine Schmid with Chan. Given the teachings of Schmid, there appears to be no motivation to incorporate the CPLD 400 of Chan as Chan does nothing to provide secure access across an untrusted PSTN. Given the teachings of Chan, one of ordinary skill in the art would appear to have no motivation to incorporate the FPGA 518 of Schmid. In particular, one of ordinary skill in the art would appear to be motivated by a low part count to program the CPLD 400 to perform the serial/parallel conversions instead of adding the cost, space and power consumed by the FPGA 518. Therefore, one of ordinary skill in the art appears NOT to be motivated to combine Chan with Schmid. As such, *prima facie* obviousness has not been established.

Furthermore, Chan and Schmid appear to be non-analogous art. Chan has a US classification of 326/41. In contrast, Schmid has a US classification of 379/189. In the absence of evidence to the contrary, the US classification system suggests that Chan and Schmid are non-analogous art. Therefore, *prima facie* obviousness has not been established. Claims 11 and 19 provide language similar to claim 1. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 2 provides two communication channels of the die coupled to two routing channels of the programmable logic device. Claim 5 provides two communication channels of the die coupled to the same (first) routing channel of the programmable logic device. Assuming, *arguendo*, that the combination of Chan and Schmid teaches

to couple two communication channels to two routing channels per claim 2 (for which Applicants' representative does not necessarily agree), the coupling of claim 5 is not taught. Assuming, *arguendo*, that the combination of Chan and Schmid teaches to couple the two communication channels to one routing channel per claim 5 (for which Applicants' representative does not necessarily agree), the coupling of claim 2 is not taught. Claims 12 and 15 provide language similar to claims 2 and 5 As such, at least two of claims 2/12 and 5/15 are fully patentable over the cited references and the rejection should be withdrawn.

Claims 3 and 4 provides three/four communication channels coupled to three/four routing channels. As argued above for claim 1, neither Chan and Schmid appear to teach coupling even one routing channel to one communication channel, let alone three/four routing channels to three/four communication channels as presently claimed. Claims 13 and 14 provides language similar to claims 3 and 4. As such, claims 3, 4, 13 and 14 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 6 provides that the first communication channel is further coupled to the first routing channel to receive a control signal from one of the logic block clusters. In contrast, both Chan and Schmid appear to be silent regarding a control signal passing from a first routing channel in the CPLD 400 of Chan (asserted similar to the claimed programmable logic device) a first communication channel in the FPGA 518 of Schmid (asserted similar to the claimed die). Furthermore, the Office Action offers no

evidence why claim 6 is allegedly anticipated by a combination of Chan and Schmid. (The Office Action arguments jump from claim 2-5 and 10 to claim 7.) As such, the Examiner is respectfully requested to either (i) provide an explanation and evidence why claim 6 is rejected or (ii) withdraw the rejection.

Regarding claims 7-9 and 16-18, the Office Action uses the same two paragraphs in the rejections:

> Each logic block 430 may be programmed to perform selected logic functions using sub-combinations of the inputs provided by the PIM 420. Thus, each cluster 410 may be regarded as a PIM coupled in series with a number of programmable logic devices coupled in parallel, wherein each logic block 430 corresponds to a single programmable logic device. Intermediate stages and the outputs of each of the programmable logic devices are fed back as inputs to the PIM 420. Depending on the particular set of input signals routed to the outputs of the PIM 420 and the programmed logic functions for each logic block 430, the individual programmable logic devices may, in fact, act as two or more programmable logic devices coupled in series with each other. Each cluster 410 thus provides a highly versatile logic device in and of itself. (Chan, column 5, lines 17-44)
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> Each output 810 for an I/O cell 700 is a dedicated line or interconnect in one of the routing channels 440 or 450. These outputs 810 may be used to provide signals to any of the clusters 410. Similarly, any of the clusters 410 may provide signals to any of the I/O cells 700 of an I/O block 800 using signal paths 820 which are also part of routing channel 440 or 450. In FIG. 8, the interconnections illustrated in area 830 show that though the use of programmable interconnections, various signals 820 may be provided to I/O cells 700. These connections perform a multiplexing function in the sense that they provide for the selection of one input conductor from a set of many input conductors. Therefore, as used in this context, the term "multiplexer" or the illustration of multiplexer in FIG. 8 should be understood to encompass any circuit that performs a multiplexing function, regardless of the number of programmable elements required to control that circuit. Preferably, the programmable elements and/or the multiplexing function may be implemented as volatile memory elements such as static random access memory. (Chan, column 7, lines 25-44)

Nowhere in the above text, or in any other section does Chan appear to mention an encoding selection signal (claim 7), a status signal (claims 8 and 17), a special character indicator (claim 9) or a control signal (claims 16 and 18). Schmid appears to be similarly silent. Claim 10 also provides a control signal. Therefore, Chan and Schmid, alone or in combination do not appear to teach or suggest an encoding selection signal, a status signal, a special character indicator and a control signal as presently claimed. As such, claims 7-10 and 16-18 are fully patentable over the cited references and the rejections should be withdrawn.

Claim 20 provides that the first communication channel is a transmit channel and the second communication channel is a receive channel associated with the transmit channel. In contrast, the Office Action admits on page 2 that Chan does not disclose a first communication channel or a second communication channel of a die. Therefore, the assertion on page 6 of the Office Action that Chan teaches characteristics of communication channels that are admitted not in the reference appears to be incorrect. Furthermore, the assertion on page 6 of the Office Action that column 4, lines 44-57 of Chan disclose characteristics of the FPGA 518 of Schmid (asserted similar to the claimed die) also appears to be incorrect. Chan teaches nothing about the FPGA 518 of Schmid. Therefore, Chan and Schmid, alone or in combination, do not appear to teach or suggest a first communication channel is a transmit channel and a second communication channel is a receive channel associated with the transmit channel as presently claimed. As

such, claim 20 is fully patentable over the cited references and the rejection should be withdrawn.

Claims 21 and 22 depend from claim 1, which is now believed to be allowable. Since the dependent claims contain all of the limitations of the independent claims, claims 21 and 22 are fully patentable over the cited references and should be allowed.

COMPLETENESS OF THE OFFICE ACTION

Aside from a notice of allowance, Applicants' representative respectfully requests any further action on the merits be presented as a **non-final** action due to incompleteness of the current Office Action. No arguments or evidence was provide for the claim 6 rejection. As such, the current Office Action is incomplete under 37 CFR §1.104(b). The Examiner is respectfully requested to include in any subsequent rejection on the merits (i) arguments and evidence for a claim 6 rejection (ii) or an allowable indication for claim 6.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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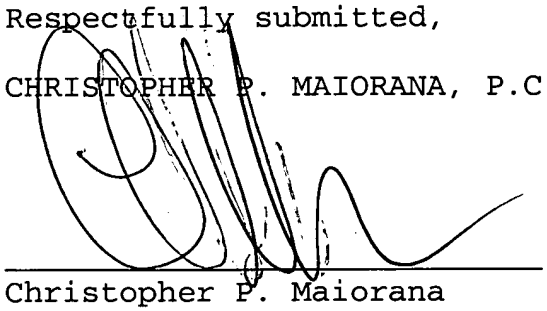

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